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RESEARCH ARTICLE

Reliability Calculation Improvement of Electrolytic Capacitor Banks Used in Energy Storage Applications Based on Internal Capacitor Faults and Degradation

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ABSTRACT Capacitor banks (CBs) play a crucial role in energy storage and frequency control within autonomous microgrids. However, the impact of internal capacitor configurations, varying in terms of equivalent series resistance (ESR), capacitance, and rated voltage, on CB degradation, reliability, and peak current remains an understudied aspect. Moreover, the absence of a capacitance degradation coefficient in the standard MIL-HDBK-217 equations for predicting the reliability of electrolytic capacitors poses a significant challenge. To address these issues, this study examines a microgrid composed of diverse renewable energy systems, featuring nine distinct CB arrangements. The design of CBs considers both capacitance and peak output current individually. An evaluation is conducted to compare construction costs, lifetimes, and peak output currents across all layouts. Additionally, a novel formula is introduced to estimate the reliability and lifetime of CBs, while an existing formula for calculating CB peak output current is enhanced. The research explores the impact of ambient temperature and capacitor voltage on the reliability of various capacitor designs, proposing a novel framework for assessing CB reliability based on MIL-HDBK-338B, which accounts for both short-circuit and open-circuit faults. The practicality of these findings is confirmed through a comparison of experimental and simulation results. The inverter operation video, simulation, and all production data including PCB and processor codes are also attached.

INDEX TERMS Power electronics, renewable energy, capacitor bank, degradation modeling, equivalent series resistance, applied mathematics, reliability analysis, energy storage.

NOMENCLATURE

A_1A_0	Area (mm^2).
C	Capacitance (F).
C_{ini}	Initial capacitance (F).
$C_{ini\ ij}$	Initial capacitance of CB in column i and row j(F).
C_{rated}	Rated capacitance of capacitor (F).
CB	Capacitor bank.
D	Diameter of internal capacitor (mm)
E	Activation energy/Boltzmann constant (4700).
E_a	Activation energy (1.4eV).
$R_{eq.P\ CB}$	PCB Equivalent resistor (Ω).
R_{ij}	ESR of capacitor in column i and row j of CB.

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R_{pcb}	Interconnection resistor of the PCB between two
R_T	capacitors.
R_{TS}	Resistance between two series capacitors (Ω).
S	Ratio of operating to rated voltage.
S_I	Distance between two pins of capacitor (mm).
R_{TC}	Resistance between terminal connector and PCB
R_{TS}	Resistance between two series capacitors (Ω).
E_a	Activation energy (1.4eV).
E_{CB}	Energy of capacitor bank (J).
$ESRo$	Initial ESR(Ω).
ESR_{CB}	Capacitor bank equivalent ESR(Ω).
ESR_{DC}DC	equivalent series resistance (Ω).
ESR_t	ESR value at the time t(Ω).
$I_{max,C\ B}$	Maximum current of capacitor bank (A).
$I_{min,C\ B}$	Minimum current of capacitor bank (A).
I_{peak}	Peak current (A).
$I_{\text{peak},t}$	Peak current at time t aging (A).
K	Boltzmann's constant (8.617E-5 eV/K).
$MTTF$	Mean Time to Failure (h).
N_P	Number of parallel capacitors.
N_S	Number of series capacitors.
$P_{d,S\ OFC}$	Difference power of SOFC (W).
P_{CB}	Capacitor bank power (W).
$R(t)$	Reliability in time t(%).
$R(t)$	Reliability at time t(h)(%).
R_{Busbar}	Interconnection resistor of the Busbar between two capacitors.
$R_{CB}(t)$	Reliability of capacitor bank at time $t(h)$(%).
$R_{CB}(t)$	Reliability of capacitor bank at time thours (%).
$R_{CB,O\ C}$	Resistance of CB in internal open circuit fault (Ω).
$R_{CB,S\ C}$	Resistance of CB in internal short circuit fault (Ω).
R_{eq}	Equivalent resistor (Ω).
S_{ij}	Ratio of operating to rated voltage of CB in column i and row j.
T	Ambient temperature (°C).
T	Time (s).
T_A	Application temperature (Celsius).
t_{aging}	Aging time (h).
T_C	Category temperature (Celsius).
V_f	Forward voltage (V).
V_i	Initial voltage (V).
$V_{operation}$	Operation voltage (V).
V_R	Rated voltage (V).
V_{rated}	Nominal rated voltage (V).
W_{CB}	Energy of the capacitor bank (J).
Δt	Time deviation (s).
λ_b	Base failure rate (Failures / $\left(10^6(\text{ h})\right)$.
λ_{CB}	Failure rate of capacitor bank (Failures / $\left(10^6(\text{ h})\right)$.
λp	Failure rate (Failures / $\left(10^6(\text{ h})\right)$
λ_{CB}	Failure rate of capacitor bank (Failures $\left(10^6(\text{ h})\right)$.
π_{CV}	Capacitance factor of a capacitor.
π_E	Environment factor.
πQ	Quality factor.
$\pi Q, i\ j$	Quality factor of CB in column i and row j.
X	X ax.
Y	Y ax.

I. INTRODUCTION

As a result of the global increase in energy consumption, reduction in fossil fuel use, and global warming, the use of renewable energy sources has become increasingly important. Photovoltaic (PV) systems are dependent on climate and geographical location, and such factors can cause problems including voltage fluctuations and frequency deviations in microgrid operation [1], [2]. Wind energy is widespread on the earth and as it involves no fossil fuel or ecological cost, it is also known as clean energy [3], [4]. When wind turbines, PV, and a fuel cell (FC) hybrid grid work together, the unwanted effects of a grid can be reduced and a clean energy system can be created, independent of the use of fossil fuel. There are several types of energy systems depending on the type of electrolyte and fuel used in FC. The solid oxide fuel cell (SOFC) type, which produces high power, is used in high power grids [5], [6]. Due to the long-time delay of FC (cold start), it is not able to quickly compensate for the variation of the load. Thus, the capacitor bank (CB) would be responsible for the fast load compensation in the transient state, and finally, SOFC compensates for the power deficit in the steady-state [7], [8]. Previous studies show that the presence of a CB enhances the frequency regulation performance of the micro-grids [9].

A. PROBLEM BACKGROUND AND THE CURRENT RESEARCH GAP

The equivalent series resistance (ESR) plays a pivotal role in constraining the peak output current of a capacitor, as evidenced by previous studies [10], [11]. Certain studies tend to overlook ESR, focusing solely on capacitance when calculating the peak power of capacitors. In reality, capacitor current is constrained by ESR. Therefore, in the design of CBs for power compensation applications, ESR must be considered to ensure the CB aligns with network requirements [12], [13], [14].

Besides the ESR and capacitance, the lifetime of the system should also be considered when designing the CBs. Capacitors degrade over time, and the CB should be designed to supply the required power to the grid in the final remaining hours of system operation [15], [16], [17], [18], [19]. However, the effects of degradation on capacitor reliability remain underexplored. While reliability relationships typ-

ically assume constant capacitor capacitance, in reality, capacitance changes over time. Therefore, for more accurate estimation, the coefficient of capacitance change over time should also be included in the reliability relations. However, the optimal series-parallel arrangement of CBs, considering cost and reliability trade-offs, remains unclear. Questions persist regarding whether a lower rated voltage or higher capacitance for internal capacitors results in the lowest cost and highest reliability.

Recent research, such as [20] and [21] investigates the future and present supercapacitor CBs technology which is useable in renewable power generation grids. These studies investigate various CB models, offering an overview of the latest publications on CB technologies and their grid applications. They focus on CBs used to control microgrid frequencies, delving into associated issues and challenges in grid integration. Reference [22] introduced a supercapacitor model which is useful for dynamic control of a power system frequency and presents a complete control strategy of CB control. Another work underscores that a simple CB model may not always suffice for frequency control in a grid [23]. This study integrates operating voltage, operating temperature, and ESR into the reliability assessment of a supercapacitor-based CB. Reference [24] introduces an improved model for estimating CB reliability, taking into account factors such as relative humidity, voltage levels, and variable temperature. A noteworthy aspect of this paper is the investigation of accelerated aging in CBs. It is worth noting that this article is a continuation of [8].

B. CONTRIBUTION AND PAPER ORGANIZATION

One notable advantage of the proposed approach over conventional artificial intelligence techniques is its ability to eliminate the need for continuous real-time measurement of capacitor parameters. By introducing a time factor into the equation, one can compute the reliability and peak current of CBs at specific intervals. The primary objectives of this study are to elucidate the impact of time on capacitive behavior. Specifically, as time progresses, the capacitance of the CBs decreases while its ESR increases. Consequently, the transient power supplied by the CB diminishes, ultimately affecting the energy stored in the CB. The study also explores the influence of temperature and voltage variations on the longevity of CBs. Evaluation of the lifespan of various real CB types is performed in accordance with relevant standards and is compared to manufacturer-provided datasheet specifications. The methodology for calculating reliability and failure rates is refined by accounting for the degradation of ESR and capacitance, with a focus on electrolytic capacitors, commonly used for CBs [25], [26], [27].

In an effort to align with practical industrial applications, this work adopts the context of a stand-alone microgrid powered by renewable energy systems. In real-world grids, capacitors inevitably experience degradation in both ESR and capacitance, making factors such as reliability, failure rates, lifespan, and output current crucial considerations. These parameters evolve over time, necessitating careful design and layout of CBs to ensure continued functionality after a specified operational duration. Therefore, a stand-alone microgrid equipped with a wind turbine, photovoltaic panels, CB, and FC is considered. The main contributions of this study can be summarized as follows:

i) Enhanced equations for capacitance and ESR, accounting for temporal changes.

ii) Novel methods for estimating the reliability and lifespan of CBs, integrating the impact of ESR and capacitance degradation.

iii) A comprehensive assessment of seven CBs with varying parameters sourced from Digikey Electronics [28], encompassing degradation and reliability analyses. The findings of this study provide practical insights for the design of capacitor banks.

iv) The research highlights that in CB design, the consideration of capacitance alone is insufficient, necessitating the inclusion of ESR and capacitor output current.

v) An investigation into the effect of degradation on the maximum output current of the capacitor bank, leading to the development of an improved time-dependent formula for output current.

vi) The introduction of new relationships for calculating PCB resistance in CBs.

vii) A comprehensive comparative analysis of cost, volume, reliability, and peak current for each CB.

The focus of this paper is to enhance the capacitance factor within the formula for calculating the reliability and lifespan of electrolytic-based CBs. Notably, the existing military standard, MIL-HDBK-217, used for assessing the reliability and lifespan of electronic components, lacks provisions for factoring in the degradation of capacitor capacitance. Instead, it assumes constant capacitance throughout a capacitor's operational life. This study, supported by extensive long-term testing, not only validates the occurrence of degradation but also quantifies its impact on various capacitor bank types available in the market. Subsequently, the coefficient derived from these analyses is integrated into calculations for reliability, lifespan, and peak current of the capacitor bank, thereby addressing a significant gap in current industry standards.

The paper is organized as follows. Section II presents the system configuration. Section III describes the aging, reliability, ESR, and capacitance of the CB. Section IV demonstrates modification in the evaluation formula of electrolytic capacitor reliability. Section V provides a discussion about degradation in reliability assessment. Limitations of the study are presented in section VII. Open questions are presented in Section VIII, and Section IX provides the conclusion of the paper.

II. SYSTEM CONFIGURATION

A. STAND-ALONE MICROGRID FEATURES

Figure 1 depicts the diagram of a renewable power system microgrid consisting of an induction generator-wind turbine

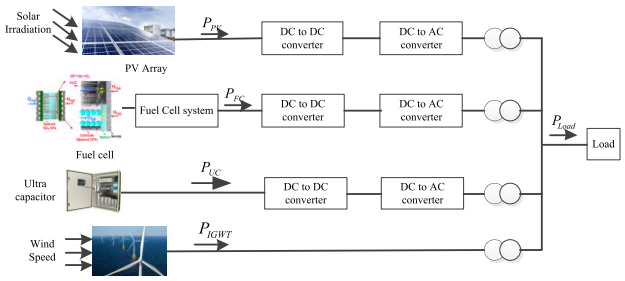


FIGURE 1. The diagram of the autonomous microgrid renewable power system.

TABLE 1. The supply/demand power of the microgrid power systems.

Item	System	Max. Power (kW)
1	Load	500
2	Wind Turbine	275
3	Photovoltaic	150
4	Fuel cell	200
5	Capacitor bank	180

(IGWT), PV, FC, CB, and load, where PV and IGWT have priority in producing power. It is possible to replace the CB with a battery or to use the battery in parallel with the CB. The point that should be considered is that in the simple case of implementing a CB bank in parallel with a battery set, the instantaneous current from each power source is inversely proportional to the internal resistances of each power source after they have stabilized in a parallel circuit. Table 1 gives the maximum load demand power and the maximum supply power of the renewable energy systems of the proposed microgrid. When the power difference between the generated power and the power consumed by the load is positive, the capacitor bank voltage increases, i.e., the excess power is supplied to the CB, and thus its voltage increases. The capacitor bank voltage decreases when the power difference turns negative or the demanded load power exceeds the generated power, meaning that the capacitor bank supplies the extra power the load needs.

In the present study, a high-order nonlinear squirrel-cage induction generator is paired with a variable-speed wind turbine. The mathematical modelling of induction generators and wind turbines is proposed in [29]. For a PV system, the simplified equivalent circuit model called the four-parameter model is employed [30]. The parameters are also according to the values given in [31]. To obtain the maximum power value, this paper used the perturbation and observation (P&O) technique [32]. A proper model of a SOFC is used in our study [33]. The SOFC compensates for the deficit power for the frequency control in steady-state time, but the transient deficit power must be compensated by the CB. Figure 2 shows the step response of the SOFC. The time difference between command and output power is 3.6 seconds. For the length of

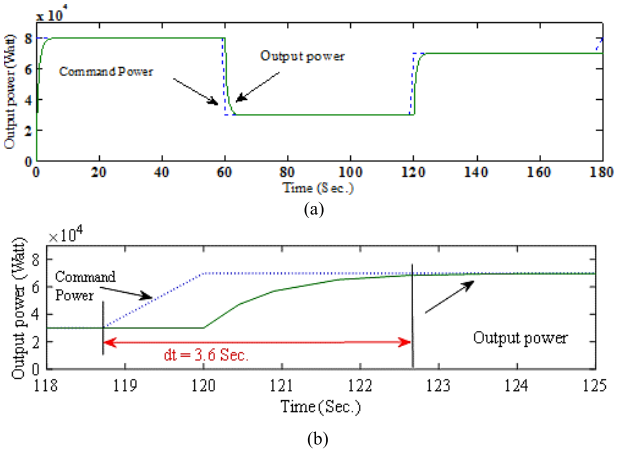


FIGURE 2. (a) The step response of the SOFC, (b) The time difference between command and output power is 3.6 seconds.

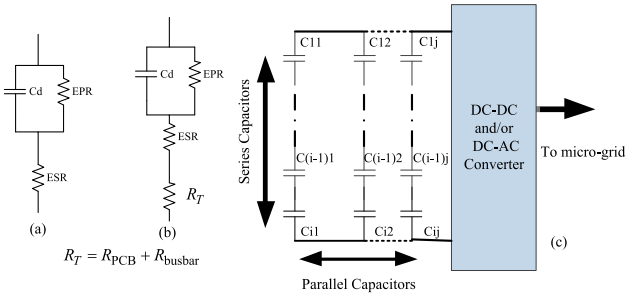


FIGURE 3. (a)Equivalent circuit of a capacitor, (b) Equivalent circuit of a capacitor consisting of trace resistor, and (c) the series-parallel combination layout of the CB.

time that the SOFC reaches full power, CB has to provide the shortage of grid power to adjust the grid frequency. Therefore, the maximum time for CB to deliver power is 3.6 seconds. Figure 3 (a) shows the equivalent circuit of an electrolytic capacitor. This model consists of the ESR, capacitance, and an EPR representing self-discharge losses. In (b), the trace resistor consisting of the printed circuit board (PCB), or busbar is added to the equivalent capacitor circuit. Different models of CB have been presented in several articles [22]. A CB acts as DC energy storage, and the amount of energy that would evaporate from the CB bank unit can be expressed as:

$$E_{\mathrm{CB}} = \frac{1}{2} C_{\mathrm{CB}} \left(V_i^2 - V_f^2 \right) \tag{1}$$

Equation (1) states that the CB bank is tasked with providing a prescribed amount of energy. When the CB releases power, the CB voltage decreases, and when the CB captures the energy, the voltage of the CB increases. The CB could be set up to construct a CB bank unit [34]. Figure 3(c) illustrates how multiple capacitor units can be arranged to construct a CB that can effectively meet the power demand of the load. Following MIL-STD-11991 [35], derating voltage for 20°C below the maximum rating should be regarded as at least 0.5. The CB voltage should not reach its maximum voltage, and

even the instantaneous voltage can damage the capacitor and cause it to fail [36].

In the realm of electronics, derating refers to the practice of operating a device at levels below its rated maximum power to enhance its lifetime. Common instances include running a component at power, current, or voltage levels below its specified maximum nominal values.

$$S = \frac{\mathrm{V_{operation}}}{\mathrm{V_{rated}}} \tag{2}$$

Thus, in the process of selecting the capacitors, the nominal voltage of the aggregate of the capacitors shall be twice the applied voltage. To comply with the derating factor, the voltage applied to the capacitor should not exceed 50% of the capacitor's rated voltage. The applied voltage of the capacitor in the microgrid is 500 V; therefore, the total permissible voltage of the capacitor bank should be at least 1000 V due to the MIL-STD-11991 standard. This significantly increases the reliability of the system. The maximum power output that the CB should be able to inject into the microgrid transiently and pulse is 180 kW. The capacitance of a CB can be computed based on the energy it holds. To calculate the capacitance, the most difficult conditions must be considered. As the discharge time of the capacitor increases, the capacitor voltage decreases, and the output current increases. The output power in the most challenging circumstances is equal to the maximum output power of the SOFC. As mentioned above, the maximum output power of the SOFC is 200 kW, and since the SOFC always provides 10% of the power due to its cold start, the power difference is going to be equal to:

$$P_{\mathrm{d,\,SOFC}} = 200\mathrm{kW} - 20\mathrm{kW} = 180\mathrm{kW} \tag{3}$$

To compute the capacitance of the capacitor bank, it is essential to specify dt, which is correlated with the SOFC step response duration of 3.6 seconds. Consequently, the total energy of the capacitor in the worst condition can be determined as follows [37]:

$$W_{SC} = \int_0^t P_{\mathrm{CB}}\mathrm{d}t = 6.84 \times 10^5(\mathrm{J}) \tag{4}$$

The relation between the CB stored energy and its capacitance is:

$$W_{\mathrm{SC}} = \frac{1}{2}C_{\mathrm{CB}}(V_1^2 - V_2^2) \tag{5}$$

Which V_1 is the Maximum allowed voltage of the CB (110% of nominal voltage = 550 V) and V_2 is the Minimum allowed voltage of the CB (15% of nominal voltage =75 V). Solving this equation results in $C_{\mathrm{CB}} = 4.6$ F.

III. AGING, RELIABILITY, ESR, AND CAPACITANCE DEGRADATION OF CB

Capacitor bank design aims to consider ESR, capacitance degradation, and CB reliability. It is attempted to show that the CB design may not be just theoretical and can be applied in industry.

A. CAPACITOR SELECTION

So far, it has been established that the capacitor bank capacitance needs to be at least 4.6 F to meet the requirements of frequency regulation. However, the most important issue in selecting a capacitor is the ESR, or internal resistance of the capacitor, which restricts the output current of the capacitor. The arrangement and selection of the capacitor should be such that the CB can supply the current required for the frequency control. If the capacitor operates at its highest voltage, the current decreases, and if the capacitor voltage falls to its lowest, more current is required to make the required power. Therefore, the maximum and minimum currents obtained by CB will be equal to:

$$I_{\mathrm{max,SC}} = \frac{180\ (\mathrm{kW})}{75\ (\mathrm{V})} = 2400\,(\mathrm{A}) \tag{6}$$

$$I_{\mathrm{min,SC}} = \frac{180\ (\mathrm{kW})}{550\ (\mathrm{V})} = 327\,(\mathrm{A}). \tag{7}$$

The conditions above must take into account not only the capacitance of the capacitor bank but also the ability of the capacitor bank to deliver the maximum current of 2400 A. To construct a CB that has both capacitances of 4.6 (F), and a voltage rating of 1000 V, a set of capacitors is assembled in series parallel. Figure 3(b) shows how the capacitor bank is arrayed.

With the series arrangement of the capacitors the CB can withstand higher voltages, and the parallel setup will increase the capacitance of the capacitor bank. The larger the number of parallel capacitors, the higher the current of the CB. For the design of the actual capacitor bank, the CBs available on the Digikey Electronics website were used to select the capacitor. The number of series (Ns) and parallel (Np) capacitors required was calculated following these equations:

$$N_S = \frac{1000V}{V_{\mathrm{rated}}} \tag{8}$$

$$N_P = \frac{4.6F}{\left(C_{\mathrm{rated}}/N_S\right)} \tag{9}$$

The resulting number is converted to the nearest larger number. For a similar comparison, all capacitors have a 20% tolerance, a radial style termination, and an operating temperature of −40 to 65°C. In selecting the capacitor, voltage, and capacitance from the market website, we tried not to choose values that are far from reality. Also, typical ESR has been kept in mind for all capacitors.

Table 2 displays different capacitors for designing a CB with 4.6 F capacitance and 1000 V nominal voltage. To check the number of multiple series-parallel states, capacitors with different nominal voltages from 10 V to 400 V were selected. This table also shows the computation of the number of capacitors depending on the capacitance of the CB. To have the same capacitor construction material in different voltages and capacitances, capacitors were selected from a random company named Illinois Capacitors [28].

Table 3 gives the current peak, which can be supplied by each CB. Following this, the maximum current demanded by

TABLE 2. The selected capacitors from Digikey [28] for CB design.

Part Number	Capacitance (μF)	Voltage (V)	NS	NP	Total CB Capacitors (NS×NP)	Diameter	Length	Volume of CB (m3)
109CKH010M	10000	10	110	50600	5,566,000	18	35.5	50.2558
688CKE016M	6800	16	69	46676	3,220,644	16	31.5	20.3874
688CKE025M	6800	25	44	29765	1,309,660	18	35.5	11.8250
108CKE100MRY	1000	100	11	50600	556,600	18	35.5	5.0256
337CKE200M	330	200	6	83636	501,816	18	40	5.1053
476CKE400M	47	400	3	293617	880,851	16	31.5	5.5760
476CKE400MQV	47	400	3	293617	880,851	16	25	4.4254

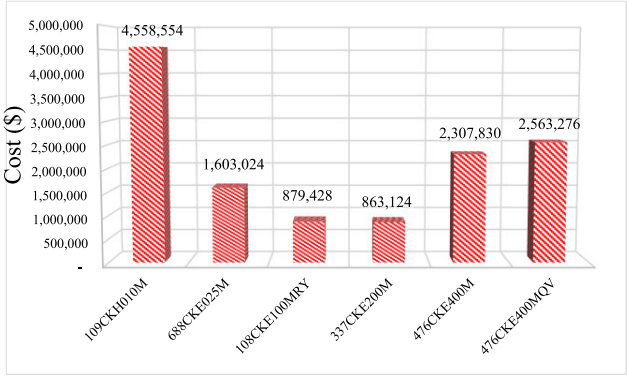


FIGURE 4. Cost Comparison of different CBs.

the microgrid is 2400 A at 75 V of the CB. Table 3 shows that CBs provide more current than is needed. To have an appropriate frequency control with a frequency deviation less than 0.01 Hz, it is essential to supply at least 2400 A at 75 V besides having a capacitance of 4.6 F. Therefore, for CBs that are not capable of delivering adequate current, the number of capacitors in parallel must be increased by dividing the number 2400 by the peak current of each capacitor.

The comparison cost curve is shown in Figure 4. From this figure, it is clear that for a CB with the same performance, the difference in cost is very significant. The design cost of the network can be greatly reduced by choosing the proper capacitor arrangement. The highest cost is for the CB arrangement using 109CKH010M, which has a total cost of $4,558,554. The 109CKH010M is a 10 V capacitor with a capacitance of 10 mF which, in a series-parallel connection, can provide the required power of 180 kW in the voltage range of 75 to 550 V. If this capacitor is used to construct the CB, the manufacturing cost will be extremely high.

In contrast, the lowest cost is related to the CB layout with 337CKE200M capacitors. This capacitor is 200 V with a capacity of 330 μF, of which 501,816 capacitors can be combined in series parallel to provide the required energy. It is also worth remembering that the thermal dynamics of power semiconductors and power capacitors are intimately related to reliability and influence the cost of power electronic converters [38].

B. RELIABILITY AND LIFETIME ESTIMATION OF THE CB

This section explores whether an increase in cost means an increase in reliability. Many component datasheets list the life of the capacitors. However, Standard 217 can also be used to calculate the probability of failure, reliability, and life of electronic components [39]. This standard is rigorous and provides a solution for evaluating the reliability of a system by assuming that the failure of one component will fail the entire system. Markov and Monte Carlo methods are methods that are used to calculate the reliability of a system more accurately [40]. In this paper, the objective is to investigate the effects of time-lapse on ESR and capacitance degradation, so standard MIL-HDBK-217 seems sufficient. The reliability parameters and variables are derived from this standard, from the subsection on reliability assessment of aluminum electrolytic capacitors. It should be noted that standard 217 is only adequate if only one CB is considered.

Equation (10) is used to assess the failure rate of aluminum, dry electrolyte polarized capacitors:

$$\lambda_p = \lambda_b \pi_{CV} \pi_Q \pi_E \tag{10}$$

where λ_p is the failure rate of the electrolytic capacitor per 10^6 (h), λ_b is the base failure rate of the electrolytic capacitor per 10^6 (h), π_{CV} is the capacitance factor of the electrolytic capacitor, π_Q is the quality factor of the electrolytic capacitor, which refers to the materials that make up the capacitor, and π_E is the environment factor of the capacitor, which refers to the environment in which this capacitor operates.

The π_{CV} and λ_b are calculated by this equation:

$$\pi_{CV} = 0.32C^{0.19} \tag{11}$$

$$\lambda_b = 0.0028\left[\left(\frac{S}{0.55}\right)^3 + 1\right]\exp\left(4.09\left(\frac{T+273}{358}\right)^{5.9}\right) \tag{12}$$

S is calculated by:

$$S = \frac{V_{\text{applied}}}{V_{\text{Nominal}}} \tag{13}$$

Based on [39], for non-military capacitors $\pi_Q = 10$ and $\pi_E = 1$ in ground-based systems. The reliability-lifetime relationship is obtained according to the following relationship [38]:

$$R(t) = e^{-\lambda t} \tag{14}$$

$$\text{MTTF} = \frac{1}{\lambda} \tag{15}$$

which MTTF is ''Mean Time to Failure''. The datasheet of some capacitors mentions the MTTF of each component.

TABLE 3. The CB layout design based on the peak output current of capacitors.

	Part Number	Max. ESR (Ω)	I_{peak} of one Capacitor (A)	I_{peak} of the CB (A)	No. of capacitors layout considering both CB ESR and capacitance
1	109CKH010M	0.063	2.03	102718	5,566,000
2	688CKE016M	0.07	1.86	86817.4	3,220,644
3	688CKE025M	0.0659	2.17	64590.1	1,309,660
4	108CKE100MRY	0.1327	1	50600	556,600
5	337CKE200M	0.754	0.675	56454.3	501,816
6	476CKE400M	7	0.217	63714.9	880,851
7	476CKE400MQV	7	0.2	58723.4	880,851

TABLE 4. Failure rate comparison of different Capacitor-banks.

Item	Part Number	The failure rate of one capacitor based on MIL-HDBK-217	The failure rate of CB (λ_{CB}) based on MIL-HDBK-338B (S_{ij}<1)
1	109CKH010M	0.022677694	0.003037
2	688CKE016M	0.021075389	0.061101
3	688CKE025M	0.021075389	0.996028
4	108CKE100MRY	0.014641949	0.05277
5	337CKE200M	0.01186087	0.048608
6	476CKE400M	0.008190256	0.000596
7	476CKE400MQV	0.008190256	0.000596

Table 5 displays the failure rate, calculated in accordance with MIL-HDBK-217, the failure rate computed using the MTTF provided in the datasheet, and the associated cost of capacitors needed for the capacitor bank. The prices referenced are sourced from the Digikey Electronics website [28].

IV. MODIFICATION IN EVALUATION FORMULA OF ELECTROLYTIC CAPACITOR RELIABILITY

A. RIGOROUS RELIABILITY ASSESSMENT BASED ON THE MIL-HDBK-217 STANDARD

In a matrix structure of capacitor banks consisting of various CBs, as illustrated in Figure 3(B), where N_s represents the number of series CBs in a row and N_P denotes the number of parallel CBs in a column, the failure rate of CB, in accordance with the rigorous MIL-HDBK-217 standard, is modified as follows:

$$\lambda_{\mathrm{CB}} = \sum_{i=1}^{N_S}\sum_{J=1}^{N_P}\left[\begin{pmatrix} 8.9376\times10^{-4}\left[\left(\frac{S_{\mathrm{ij}}}{0.55}\right)^3+1\right] \\ \exp\left(4.09\left(\frac{T+273}{358}\right)^{5.9}\right)\end{pmatrix}\times C_{\mathrm{ini,ij}}^{0.19}\exp\left(-3.8\times10^{-6}t\right)\pi_{\mathrm{Q,ij}}\pi_E\right] \tag{16}$$

This also improves the formula for evaluating capacitor bank reliability according to the following equation:

$$R_{\mathrm{CB}}(t) = \prod_{i=1}^{N_S}\prod_{j=1}^{N_P} \times \exp\left[\begin{pmatrix} -8.9376\times10^{-4}\left[\left(\frac{S_{\mathrm{ij}}}{0.55}\right)^3+1\right] \\ \exp\left(4.09\left(\frac{T+273}{358}\right)^{5.9}\right)\end{pmatrix}\times C_{\mathrm{ini,ij}}^{0.19}\exp\left(-3.8\times10^{-6}t\right)\pi_{\mathrm{Q,ij}}\pi_E t\right] \tag{17}$$

The MIL-HDBK-217 standard assumes that if one component of a module fails, the entire module fails, which is why this standard is called rigorous.

B. RELIABILITY ASSESSMENT BASED ON MIL-HDBK-338B

Based on MIL-HDBK-338B [41], all fault types should be considered for reliability assessment, including short circuit and open circuit faults. When an open circuit occurs, the internal capacitor disconnects from the other capacitors, so that the entire column in CB is disconnected. In other words, the more the columns, the more reliability, but within the column, the more series capacitors mean a higher probability of failure. If the identical internal capacitors may fall into open circuit faults, the following reliability relationship is obtained for a CB:

$$R_{\mathrm{CB,OC}} = 1-\prod_{j=1}^{N_P}\left(1-\prod_{i=1}^{N_S}\left(1-R_{\mathrm{ij}}(t)\right)\right) \tag{18}$$

In the event of a short circuit, the ESR of the internal capacitor is sustained. In other words, the corresponding column of the CB does not get disconnected. Instead, the voltage of the CB is distributed among the other capacitors in the relevant column. Consequently, the reliability relationship of the CB can be expressed as follows:

$$R_{\mathrm{CB,SC}} = \prod_{j=1}^{N_P}\left(1-\prod_{i=1}^{N_S}\left(1-R_{\mathrm{ij}}(t)\right)\right) \tag{19}$$

Therefore, the reliability of the capacitor bank will be as follows:

$$R_{\mathrm{CB}} = R_{\mathrm{CB,OC}} + R_{\mathrm{CB,SC}} - \left(R_{\mathrm{CB,OC}}\times R_{\mathrm{CB,SC}}\right)$$

TABLE 5. The effect of 10°C rises on the MTTF of different capacitors.

	Part Number	failure rate at 20°C	failure rate at 30°C	MTTF ($\times 10^6$ h) at 20°C	MTTF ($\times 10^6$ h) at 30°C
1	109CKH010M	0.0227	0.0307	44.10	32.57
2	688CKE016M	0.0211	0.0285	47.45	35.09
3	688CKE025M	0.0211	0.0285	47.45	35.09
4	108CKE100MRY	0.0146	0.0198	68.30	50.51
5	337CKE200M	0.0119	0.0160	84.31	62.50
6	476CKE400M	0.0082	0.0111	122.10	90.09
7	476CKE400MQV	0.0082	0.0111	122.10	90.09

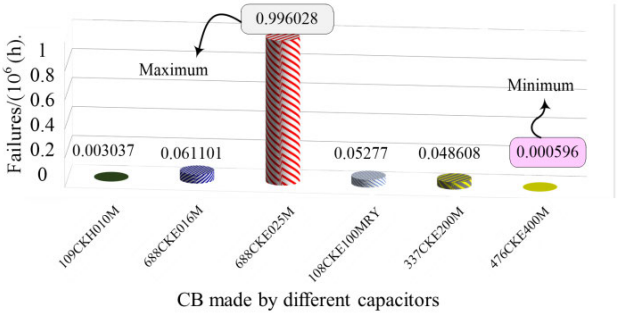


FIGURE 5. Failure rate comparison of all CBs.

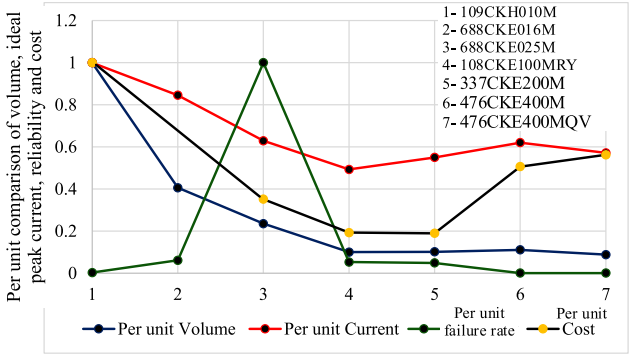


FIGURE 6. Comparison of volume, peak current, reliability, and cost of all CBs per unit.

$$= \left\{ \begin{array}{l} \left[\begin{array}{l} -\left(1-\prod_{j=1}^{N_P}\left(1-\prod_{i=1}^{N_S}\left(1-R_{ij}(t)\right)\right)\right)\times \\ \left(\prod_{j=1}^{N_P}\left(1-\prod_{i=1}^{N_S}\left(1-R_{ij}(t)\right)\right)\right) \end{array} \right] + \\ \left(1-\prod_{j=1}^{N_P}\left(1-\prod_{i=1}^{N_S}\left(1-R_{ij}(t)\right)\right)\right)+ \\ \left(\prod_{j=1}^{N_P}\left(1-\prod_{i=1}^{N_S}\left(1-R_{ij}(t)\right)\right)\right)- \end{array} \right\} \tag{20}$$

Table 4 and Figure 5 show the failure rate comparison of all CBs. The lifetime predictions of CBs were made by assuming a temperature of 20°C, a lower quality type, and a ground application.

The highest failure rate relates to 688CKE025M. Although this capacitor belongs to the CB classification, it is not recommended for use in this grid. The highest hourly failure rate of this capacitor bank is equal to 0.99. This number means that the entire CB is expected to fail in 1,000,000 hours. The lowest failure rate is related to 476CKE400M. The degradation of the capacitance and the ESR of the CB over time will be investigated next.

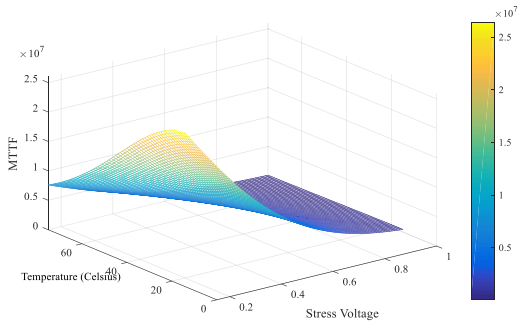
Figure 6 shows a general comparison between CBs made with different capacitors. These comparisons include the failure rate, CB volume, peak current, and cost of each CB. It is clear from Figure 6 that the highest cost, volume, and current are associated with lower voltage and higher capacitance capacitors, but the best reliability is with the higher voltage and lower capacitance capacitor. The only thing that can be mentioned with certainty is that as the internal capacitor voltage increases, the CB volume decreases. From this figure, it can be deduced that when designing a CB, a balance must exist between all the parameters to obtain the best response, and this balance depends on the state of the system or grid in which the CB is used.

C. EFFECTS OF TEMPERATURE ON CB RELIABILITY AND MTTF

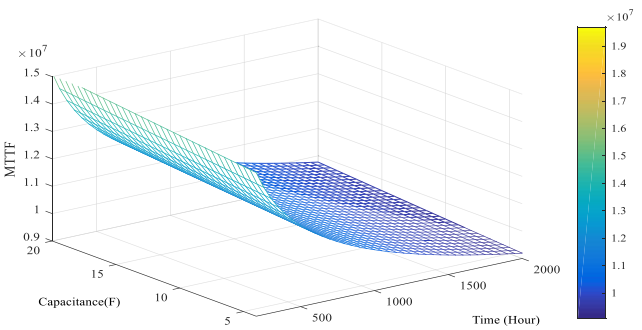
The effect of temperature on the CB lifetime can be investigated using (12) [39]. The reliability assessment is initially conducted at a temperature of 20°C. Subsequently, to examine the impact on failure outcomes, the temperature is raised by 10°C, with a corresponding consideration of a voltage stress factor of 0.5 in the equation. Table 5 illustrates the effect of a 10°C temperature rise on the MTTF for various CBs. It provides insights into the correlation between the increase in temperature, voltage stress, and the resultant decrease in MTTF for a mere 10°C temperature elevation. The conclusion may be drawn that grid design should try to reduce the ambient temperature as much as possible.

D. EFFECTS OF THE STRESS VOLTAGE ON THE ELECTROLYTE CAPACITOR RELIABILITY AND LIFETIME

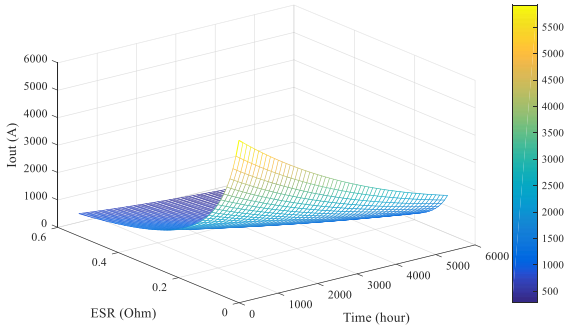
Throughout the entire section, it is assumed that the ambient temperature is 20°C, and the voltage stress is reduced from 0.5 to 0.4. This reduction implies that the applied voltage on the electrolytic capacitor, initially assumed to be 500 V, will now increase to 400 V. As voltage increases, reliability and lifetime decrease, and the failure rate rises. Table 6 delineates



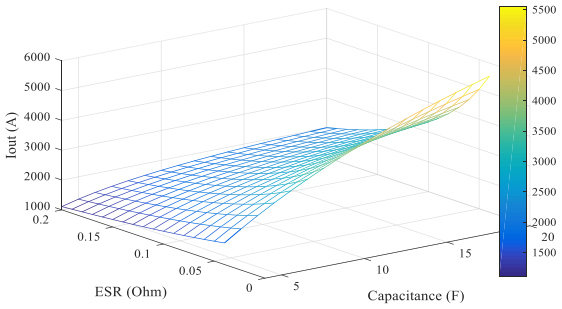
(a) The effects of temperature and stress voltage on the MTTF of the CB.



(b) The effect of capacitance degradation on MTTF of the CB over time.



(c) The effect of ESR degradation on the output current under constant 4.6 F capacitance of CB.



(d) The effect of Capacitance and ESR of CB on the output current.

FIGURE 7. The effect of ESR degradation on the output current under constant 4.6F capacitance of CB.

TABLE 6. The effect of voltage reduction on the MTTF and failure rate of CB.

	Part Number	Failure Rate at 20°C, S=0.5	Failure rate at 20°C, S=0.3	MTTF (×106 h) at 20°C, S=0.5	MTTF (×106 h) at 20°C, S=0.3
1	109CKH010M	0.0227	0.0147	44.05	68.03
2	688CKE016M	0.0211	0.0136	47.39	73.53
3	688CKE025M	0.0211	0.0136	47.39	73.53
4	108CKE100MRY	0.0146	0.0095	68.49	105.26
5	337CKE200M	0.0119	0.0077	84.03	129.87
6	476CKE400M	0.0082	0.0053	121.95	188.68
7	476CKE400MQV	0.0082	0.0053	121.95	188.68

the impact of reducing capacitor voltage on MTTF and the failure rate of the capacitor. A lower voltage drop corresponds to an extended capacitor lifetime, implies a reduction in the failure rate. In Figure 7(a), the effects of temperature and voltage stress on the MTTF of the capacitor are depicted. Additionally, Figure 7(b) illustrates the influence of capacitance degradation on the MTTF of the CB over time. It is noteworthy that previous reliability assessments did not consider the effect of degradation.

According to (44), Figure 7(c) shows the effect of ESR degradation on the output current at a constant CB capacitance of 4.6 F. Temperature and voltage are taken into account at 25 °C and 1000 V, respectively. It is observed that the ESR increases over time and consequently the peak output current ability of the CB also decreases. At constant time, it may be observed that the lower the ESR of a capacitor is, the higher its output current is. According to (16), Figure 7(d) also shows the output current curve with the variable's capacitance and ESR at constant time. The considered voltage is 1000 V, the temperature is 25 °C, and the capacitance is between 4 and 20 F in the 150th hour of operation. One may notice the effectiveness of the low ESR in the current.

E. EFFECT OF PCB RESISTOR IN PEAK CURRENT OF THE CB

The distribution of DC current in PCBs and busbars imposes limits on the flowing current, contingent upon factors such as the thickness of the PCB or busbar, the distance between two series capacitors, and the effective width of the flowing current. The reduction of path resistance is influenced by the number of output connectors; more connectors result in lower

TABLE 7. Resistance per meter of copper conductors at 20°C.

	Conductor cross-sectional area (mm^2)	Resistance per meter ($m\Omega/m$)
1	1.0	18.1
2	1.5	12.10
3	2.5	7.41
4	4.0	4.61
5	6.0	3.08
6	10.0	1.83
7	16.0	1.15
8	25.0	0.727

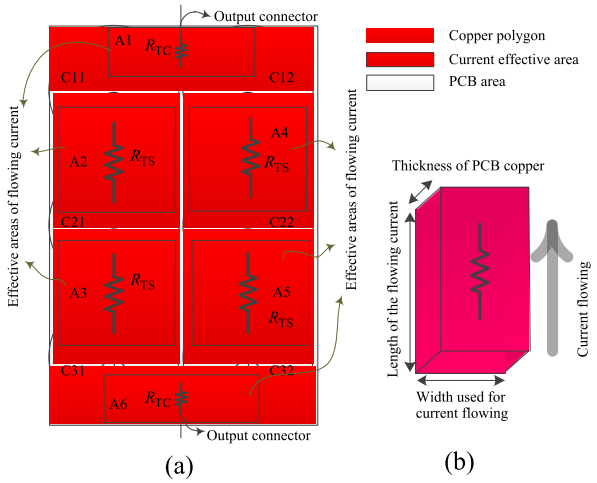
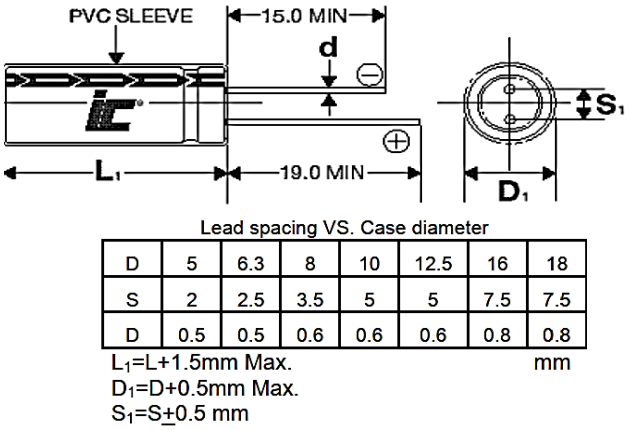


FIGURE 8. Effect of PCB resistance on CB current flow, (a) an example of modified CB current calculation with 2 × 3 capacitors, (b) PCB resistance 3D scheme.



Lead spacing VS. Case diameter

D	5	6.3	8	10	12.5	16	18
S	2	2.5	3.5	5	5	7.5	7.5
D	0.5	0.5	0.6	0.6	0.6	0.8	0.8

L_1=L+1.5mm Max. mm
D_1=D+0.5mm Max.
S_1=S±0.5 mm

FIGURE 9. Definition of diameter (D_1) and distance between positive and negative pins (S_1) of the capacitor.

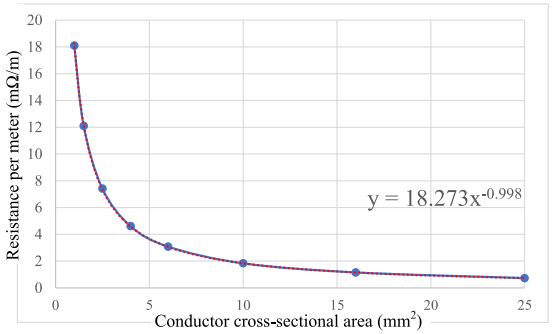


FIGURE 10. The relation between conductor cross-sectional area and resistance per meter.

resistance. Table 7 provides an overview of the resistance per meter of copper conductor at 20°C [42]. In low-voltage applications, the PCB is responsible for conducting the current of the CB, while in medium and high-voltage applications, busbars are employed for current conduction.

Figure 8 shows an example of a capacitor bank containing 6 capacitors. There are two columns, each containing three capacitors in series. There is a PCB resistor between every two capacitors, and the terminal connector pads are shown at the bottom and top of the capacitor bank. The PCB should be coated with a polygon of copper to achieve minimum resistance. Figure 8(a) shows the copper polygon, the PCB area, and the effective area for current flow in different colors. The effective area for the flowing current is considered with the help of [43] and [44].

In reality, based on Figure 9 [28], the distance between the positive and negative pins of the capacitor (S1) in terms of the diameter of the capacitor (D1) is not constant at different voltages and capacitances and varies approximately between 0.4 and 0.5, thus, the most rigorous condition is assumed for considering the maximum resistance in the current path:

$$A_{2,3,4,5} \approx 2\frac{D_1 - S_1}{2} \times D_1 = D_1(D_1 - S_1) \qquad (21)$$

$$A_{1,6} \approx D_1 \times \frac{D_1 - S_1}{2} \qquad (22)$$

Figure 8(b) shows the trace of the PCB, and in (21)-(22), D1 is the length of the flowing current, and (D1-S1) is the width of the flowing current. If the PCB contains two copper layers, the intended copper areas are parallel to each other, resulting in half the resistance of the conductive path, and therefore:

$$A_{2,3,4,5} \approx D_1(D_1 - S_1)/2 \qquad (23)$$

$$A_{1,6} \approx D_1 \times \frac{D_1 - S_1}{4} \qquad (24)$$

Figure 10 illustrates the curve and the relationship between the conductor cross-sectional area and the resistance per meter.

The relationship between conductor cross-sectional area and resistance per meter can be expressed as follows:

$$R_{CCS} = 18.273\,(L_c)^{-0.998} \qquad (25)$$

The copper volume in each layer through which the current flows is calculated as follows:

$$\text{Volume} = \text{width} \times \text{lenght} \times \text{thickness}$$
$$\Rightarrow V_{2,3,4,5} = (D_1 - S_1) \times h \qquad (26)$$

TABLE 8. Comparison of CB peak output currents under ideal conditions and considering PCB resistance at different copper thicknesses.

Part Number	Ideal I_{peak} of the CB (A)	I_{peak} of the CB considering PCB resistance (1oz copper thickness) (A)	I_{peak} of the CB considering PCB resistance (3oz copper thickness) (A)	I_{peak} of the CB considering PCB resistance (6oz copper thickness) (A)
109CKH010M	102,718	96,868.2	100,686.4	101,690.0
688CKE016M	86,817.4	84,171.8	85,915.0	86,362.7
688CKE025M	64,590.1	62,986.0	64,044.9	64,315.5
108CKE100MRY	50,600	50,462.2	50,553.8	50,576.7
337CKE200M	56,454.3	56,402.3	56,436.9	56,445.4
476CKE400M	63,714.9	63,708.0	63,712.6	63,713.7
476CKE400MQV	58,723.4	58,717.6	56,815.4	58,722.4

$$V_{1,6} = D_1 \times \frac{D_1 - S_1}{2} \times h \tag{27}$$

Hence, the trace resistance in one layer between the two series resistances in each column of the CB can be calculated as follows:

$$R_{\text{TS,one layer}} = 18.273\,(hD_1)^{-0.998}\,(D_1 - S_1) \tag{28}$$

If the PCB features a double copper layer, the polygons of the double-layer traces run parallel to each other, resulting in the halving of the resistance value, as follows:

$$R_{\text{TS}} = 9.14\,(hD_1)^{-0.998}\,(D_1 - S_1) \tag{29}$$

Also, the resistance of the connector in a two-layer PCB is as follows:

$$R_{\text{TC}} = 9.14\left(h\left(2\frac{D_1}{2}\right)\right)^{-0.998}\left(\frac{(D_1 - S_1)}{2}\right) \tag{30}$$

Therefore, the equivalent resistance of the CB shown in Figure 8(a) will be as follows:

$$R_{\text{eq}} = [(R_{\text{TS}} + R_{\text{TS}}) \,||\, (R_{\text{TS}} + R_{\text{TS}})] + R_{\text{TC}} + R_{\text{TC}} \tag{31}$$

$$R_{\text{TC}} \approx \frac{1}{2}R_{\text{TS}} \Rightarrow R_{\text{eq}} = ((3-1)R_{\text{TS}}) \,||\, ((3-1)R_{\text{TS}}) + 2R_{\text{TC}} \tag{32}$$

$$R_{\text{eq}} = \frac{((3-1)R_{\text{TS}})}{(2)} + 2R_{\text{TC}} \tag{33}$$

Finally, considering equations (21) to (33), the following equation is obtained for calculating the equivalent resistance of the CB:

$$R_{\text{eq,PCB}} = \frac{((N_S - 1)R_{\text{TS}})}{(N_P)} + 2R_{\text{TC}} \tag{34}$$

$$R_{\text{eq,PCB}} = \frac{\left(9.14(N_S - 1)(D_1 - S_1) \times (hD_1)^{-0.998}\right)}{(N_P)} + \left(9.14(D_1 - S_1)\left(h\left(N_P\frac{D_1}{2}\right)\right)^{-0.998}\right), N_P > 1 \tag{35}$$

F. ESR AND CAPACITANCE DEGRADATION

The previous section explained why the maximum current of the capacitor is extremely important. The relationship between the maximum output current of the capacitor based on its nominal voltage is as follows [45]:

$$I_{\text{peak}} = \frac{\frac{1}{2}V_R}{\frac{\Delta t}{C_{\text{CB}}} + \text{ESR}_{\text{CB}}} = \frac{1}{2}\frac{C_{\text{CB}}V_R}{\Delta t + \text{ESR}_{\text{CB}} \times C_{\text{CB}}} \tag{36}$$

In these capacitor datasheets, the capacitor's peak current is calculated using dt = 0.01 s. Thus, the (36) becomes the following relationship:

$$I_{\text{peak}} = \frac{\frac{1}{2}V_R}{\frac{1}{C} + \text{ESR}_{\text{CB}}} = \frac{1}{2}\left(\frac{C_{\text{CB}}V_R}{0.01 + \text{ESR}_{\text{CB}} \times C_{\text{CB}}}\right) \tag{37}$$

Considering the PCB/Busbar resistance of (35), the peak current of the CB would be:

$$I_{\text{peak}} = \frac{C_{\text{CB}}V_R}{2} \times \left[\Delta t + \left(\frac{\text{ESR}_{\text{CB}} + \frac{\left(9.14(N_S-1)(D_1-S_1)\times(hD_1)^{-0.998}\right)}{(N_P)}}{+\left(9.14(D_1 - S_1)\left(h\left(N_P\frac{D_1}{2}\right)\right)^{-0.998}\right)}\right)\right]^{-1} \times C_{\text{CB}} \tag{38}$$

Therefore, the peak current of each CB is shown in Table 8 and Figure 11 based on (38), considering the different PCB resistances and the maximum ESR at the frequency of 120 (Hz) and temperature of 20 °C. The total losses under peak current conditions are shown in Table 9 and Figure 12.

Table 8 and Figure 11 present a comparison of the peak output currents of the CBs under ideal conditions and when considering the PCB resistance at various copper thicknesses. The CB's capability to deliver more current increases with the augmentation of copper thickness. The PCB resistance acts as a constraint on the CB's output current, and its escalation results in increased losses, as depicted in Table 9 and Figure 12. It is noteworthy that the capacitance and ESR of the capacitors undergo changes over time [45], [46]. The objective is to identify how the output current of each capacitor varies over time. The following formula shows the ESR

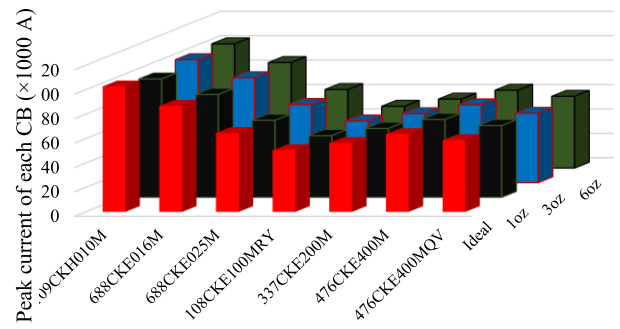


FIGURE 11. Comparison of CB peak currents under ideal conditions and considering PCB resistance at different copper thicknesses.

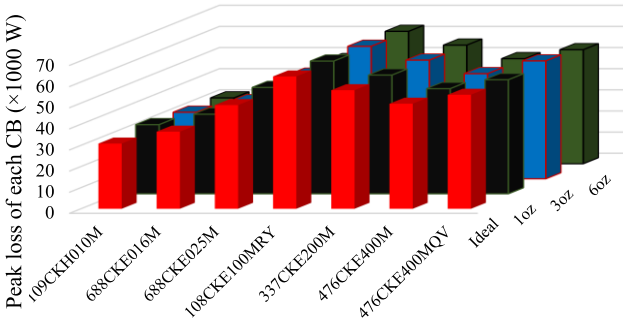


FIGURE 12. Total losses of the CBs at their maximum currents considering the PCB resistance at different copper thicknesses.

degradation:

$$\frac{1}{\mathrm{ESR}_t} = \frac{1}{\mathrm{ESR}_0}\left(1 - k.t.\exp\left(\frac{-E}{T+273}\right)\right) \tag{39}$$

therefore:

$$\mathrm{ESR}_t = \frac{\mathrm{ESR}_0}{\left(1 - k.t.\exp\left(\frac{-E}{T+273}\right)\right)} \tag{40}$$

The CBs consist of configurations that are assemblies of series-parallel electrolyte capacitors. Given the analogous nature of the performance of electrolyte capacitors, it becomes possible to estimate the performance of other electrolyte capacitors by scrutinizing the practical and laboratory performance of a single electrolyte capacitor. Although this estimation might not be pinpoint accurate, it closely reflects reality. Therefore, the performance of other electrolyte capacitors can be probed by approximating the performance of a representative electrolyte capacitor.

In the study documented in [45] experimentation was conducted on an electrolyte capacitor, tracking the variation in capacitance over time. Figure 16 depicts the capacitance degradation curve of this specific capacitor. The Y-axis represents the percentage of the capacitor's capacitance, while the X-axis corresponds to time (hours).

V. EXPERIMENTAL RESULTS

A capacitor bank may consist of a series-parallel combination of electrolytic capacitors [47], [48], [49], [50], [51]. It is possible to use aluminum electrolytic capacitors to build a capacitor bank. Therefore, we selected an aluminum electrolytic capacitor (UVY1H102MHD1TO), and then by connecting four capacitors in parallel, we proposed a capacitor bank as an energy storage device on a smaller scale. With the aim of extrapolating the results to a real capacitor bank, a practical experiment was undertaken on a smaller scale to examine the degradation of capacitor capacitance over time and derive a corresponding formula. Following (5), the energy stored in the capacitor can be computed using the capacitance of the capacitor; hence, practical experiments were conducted to measure only the capacitance of the capacitor. In this experiment, the capacitance of four 50V capacitors used in a multi-level inverter [52] was investigated.

The applied voltage of these capacitors was 24 V, which was recorded as the result of capacitance degradation over 150 h. UVY1H102MHD1TO is the component number of the capacitors under test, which were inserted into the circuit in parallel. The results of the capacitance degradation were recorded every 50 h. Before assembly, the capacitance of the capacitors was measured, and every 50 h capacitors were disassembled, and their capacitance was measured and recorded individually.

Figure 13(a) displays the prototype configuration of the multi-level inverter, featuring an experimental test conducted on a reduced switched 13-level multi-level inverter as published in [52]. Within this figure, the four capacitors, denoted as switched capacitors and arranged to form a square, have undergone capacitance measurement and recording over a 2000-hour duration. It's noteworthy that detailed information regarding the experimentally tested aluminum capacitors is as follows: Rated Capacitance is 1000 μF, Rated Voltage is 50 V, Rated Ripple is 950 mA RMS at 105°/120Hz, and the leakage current is 500 μA at 20° after 2 minutes. Figure 13(b) provides a visual representation of the four capacitors that were assembled and disassembled for capacitance measurement. The paper includes attached images showcasing the captured capacitance measurements for all capacitors. The video depicting the correct operation of the inverter is also attached to the article. Figure 14 displays the current and voltage of the experimental test capacitors. These capacitors are connected in parallel. Its voltage is around 24 V and the peak transient current is close to 20 A in 700 microseconds. Figure 15 showcases the measurement of capacitance values for four capacitors, while Table 10 details the capacitance measurements of these capacitors. The outcomes reveal a degradation in the average capacitance of the selected capacitors over time. Furthermore, Table 11 provides a representation of the percentage decrease in the measured capacitances.

The four capacitors that were measured and recorded over 2000 hours are shown in Figure 9. The images shown in Figure 9 are four sample measurements for each capacitor. Due to the large number of images that could not be included

TABLE 9. Total losses of the CBs at their maximum currents considering the PCB resistance at different copper thicknesses.

Part Number	Ideal loss (W)	Loss of 1oz copper thickness (W)	Loss of 3oz copper thickness (W)	Loss of 6oz copper thickness (W)
109CKH010M	30,842	32,704	31,464	31,154
688CKE016M	36,490	37,637	36,874	36,683
688CKE025M	49,048	50,297	49,465	49,257
108CKE100MRY	62,609	62,780	62,666	62,638
337CKE200M	56,116	56,168	56,133	56,125
476CKE400M	49,721	49,727	49,723	49,722
476CKE400MQV	53,948	53,953	55,760	53,949

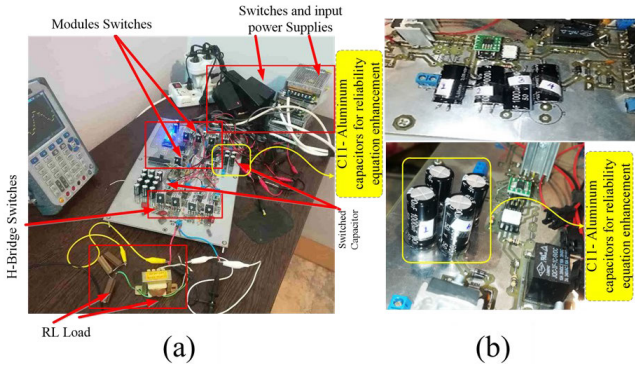


FIGURE 13. (a) the prototype configuration of the multi-level inverter, (b) four capacitors that were assembled and disassembled for capacitance measurement.

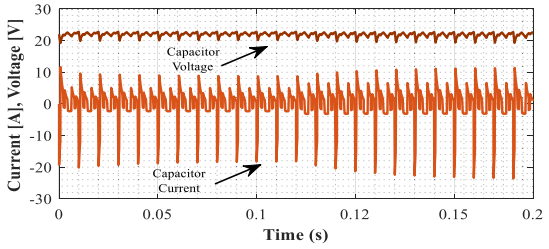


FIGURE 14. The current and voltage of the experimental test capacitors.

FIGURE 15. Measurement of the capacitance values of four capacitors.

in the article, we have placed some sample images in Figures 7 and 9 and have included the rest of the images as supplementary documents to the article.

Figures 17 and 18 illustrate curves depicting capacitance degradation per Farad unit and the corresponding percentage reduction. The reduction rate of capacitor capacitance is then compared with the improvement proposed in Equation (42), derived from the average degradation capacitance of the tested capacitors. Additionally, Figure 16 consolidates the average outcomes from Figure 17 and those obtained from

TABLE 10. The capacitance of the measured capacitors.

Time (h)	Cap. No.1 (μF)	Cap. No 2 (μF)	Cap. No 3 (μF)	Cap. No 4 (μF)
0	978	1002	993	965
50	970	995	987	956
100	965	990	985	954
150	963	987	977	949
200	959	983	970	945
400	950	974	959	937
600	943	966	950	931
800	937	960	946	925
1000	934	956	942	922
1200	929	950	938	920
1400	928	949	936	918
1600	927	948	935	917
1800	927	947	934	916
2000	923	945	930	913

TABLE 11. The percentage reduction of selected capacitances.

Time (h)	Cap. No.1 (μF)	Cap. No 2 (μF)	Cap. No 3(μF)	Cap. No 4 (μF)
0	0	0	0	0
50	-0.77	-0.7	-0.6	-0.88
100	-1.36	-1.2	-0.81	-1.1
150	-1.51	-1.5	-1.61	-1.6
200	-1.9	-1.89	-2.31	-2.07
400	-2.85	-2.83	-3.42	-2.82
600	-3.54	-3.64	-4.32	-3.47
800	-4.15	-4.19	-4.74	-4.05
1000	-4.52	-4.63	-5.15	-4.36
1200	-5	-5.15	-5.53	-4.65
1400	-5.1	-5.24	-5.77	-4.81
1600	-5.17	-5.36	-5.81	-4.94
1800	-5.23	-5.46	-5.96	-5.02
2000	-5.65	-5.7	-6.3	-5.31

reference [46] into a single curve. Through interpolation, two types of formulas, one exponential and one polynomial, can be derived. The 4th order polynomial formula exhibits the most robust response, albeit being a larger and more complex relationship. The slope of these two formulas and their trajectory progresses in the same direction over time, and with a slight differential, they yield relatively similar results.

Using the graph in Figure 17, the accurate (41) and (42) can be extrapolated.

$$Y = (2E - 13x^4) - (2E - 09x^3) + (6E - 06x^2) - (0.0087x) + 99.984, \quad (41)$$

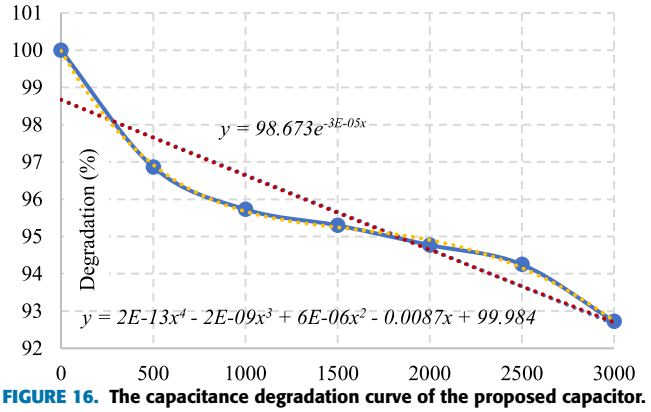


FIGURE 16. The capacitance degradation curve of the proposed capacitor.

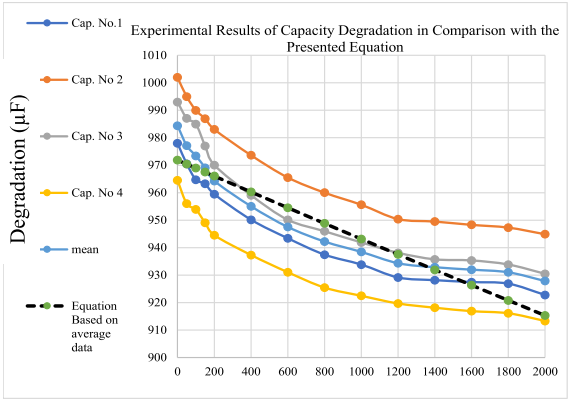


FIGURE 17. The capacitance degradation curves per Farad.

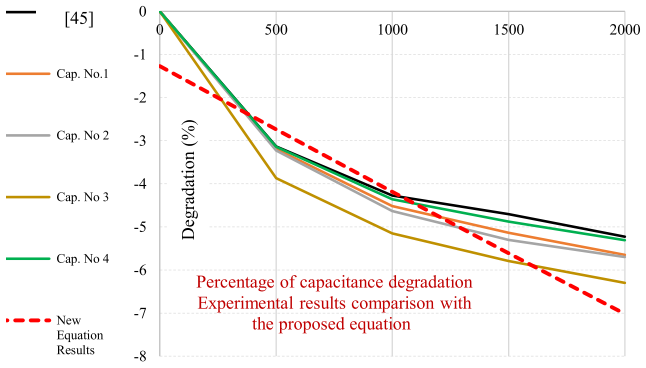


FIGURE 18. The percentage of capacitance reduction.

where y is the percentage of capacitance and x is the time in hours. Equation (41) is too large and a reduced equation makes the following equations more straightforward, therefore the exponential (42) is used for the following calculation. For an approximate estimate of the output current related to degradation, (42) is appropriate. For greater accuracy, (41) may be used instead of (42), into (43).

$$C_t = C_{\text{ini}} 0.98673 \exp(-3t \times 10^{-5}) \tag{42}$$

Figure 18 depicts the percentage degradation of capacitance in experimental results compared to the suggested equation. The black line represents the degradation rate

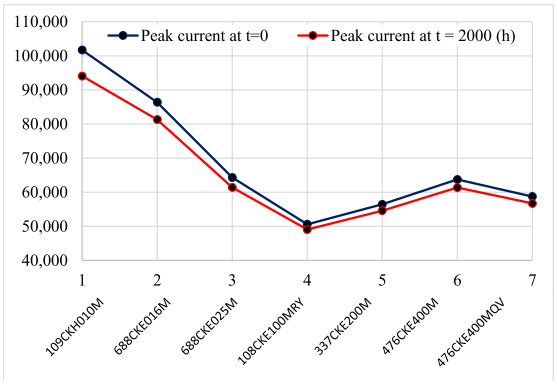


FIGURE 19. The Max. CB current deliverable after 2000 hours (f=100 Hz).

from [46], while the red dotted line illustrates the comparison of the presented formula with the experimental results. The findings in Figure 18 indicate that the measured values align closely with the experimental results from [46]. The figures show that the capacity decreases over time and consequently the amount of energy that the capacitor can store also decreases, thus this decrease in capacity in the grid must be considered. Through the (36), (40), (42) and the following relation is obtained:

$$I_{\text{peak,t}} = \frac{1}{2} \frac{0.98673 C_{\text{ini}} \exp\left(-3t_{\text{aging}} \times 10^{-5}\right) V_R}{1 + \frac{(\text{ESR}_0 + R_{\text{PCB}}) \times 0.98673 C_{\text{ini}} \exp\left(-2t_{\text{aging}} \times 10^{-5}\right)}{\left(1 - k.t. \exp\left(\frac{-E}{T+273}\right)\right)}} \tag{43}$$

$$I_{\text{peak,t}} = \frac{\frac{1}{2}\left(1 - k.t. \exp\left(\frac{-E}{T+273}\right)\right) C_{\text{ini}} 0.98673 \exp(-2t_{\text{aging}} \times 10^{-5}) V_R}{\left(1 - k.t. \exp\left(\frac{-E}{T+273}\right)\right) + \left((\text{ESR}_0 + R_{\text{PCB}}) C_{\text{ini}} 0.98673 \exp(-3t_{\text{aging}} \times 10^{-5})\right)}. \tag{44}$$

Figure 19 displays the maximum CB current deliverable after 2000 h. Since each CB has a different ESR, they also exhibit different degradation after 2000 h and their maximum output current is different from each other.

The lower the CB current, the smaller the allowable voltage range of the capacitor for charging and discharging. According to (5), as the capacitor capacitance decreases, the energy stored in the capacitor also decreases, and two main events will result: a) less energy is stored from IGWT and PV, and b) at lower voltages, the ability to inject the required power will decrease and the frequency response will be weaker. The result of this equation is that when designing a capacitor bank for the grid, significant attention needs to be devoted to the CB operating age, lifetime, and degradation factors of each capacitor.

The content of the capacitor degradation topic differs from the capacitor reliability topic. MTTF is the capacitor's mean

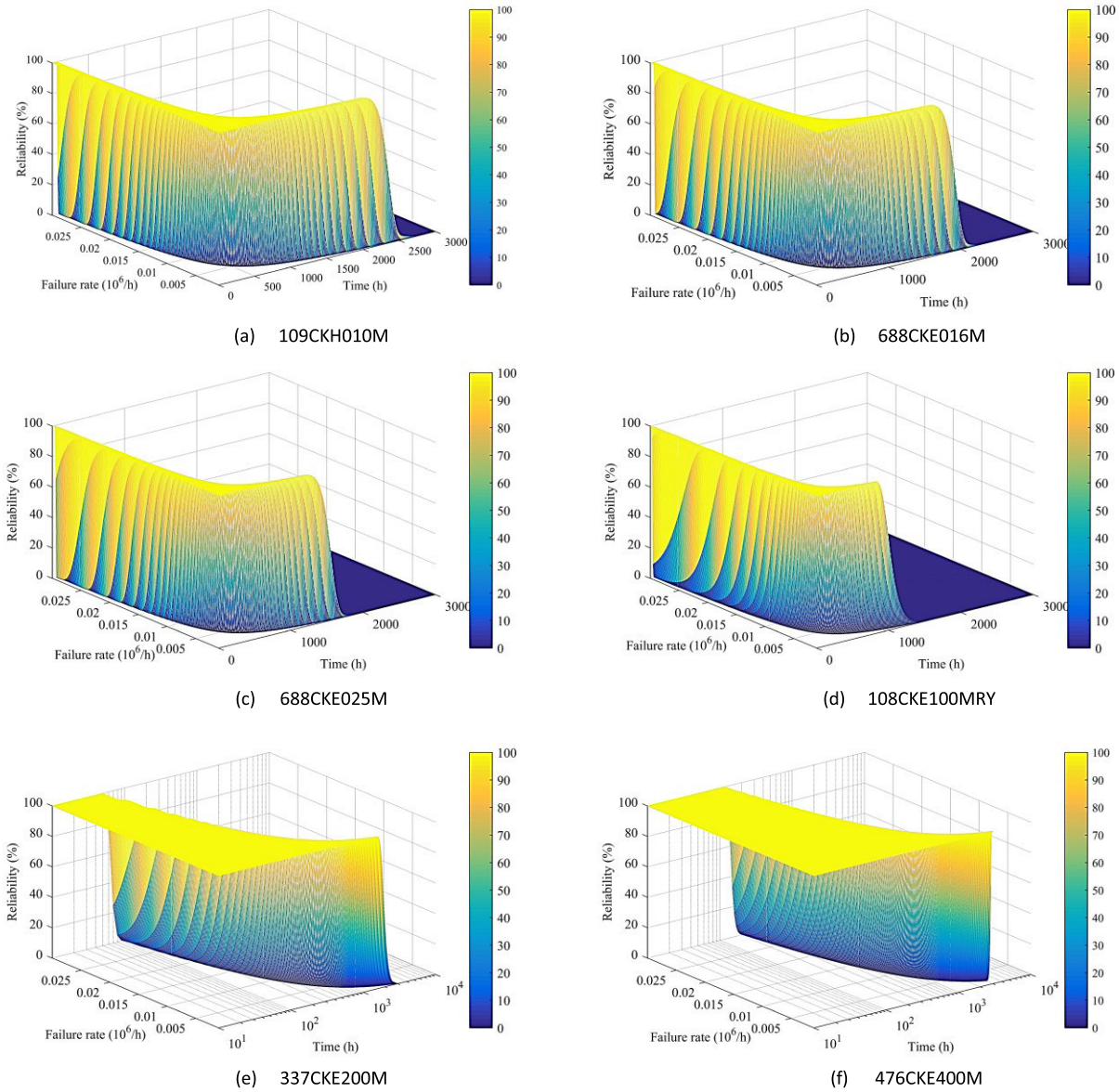


FIGURE 20. The effects of failure rate (including degradation) and time on the reliability of the capacitor banks composed of different electrolytic capacitors, the CBs made by (a) 109CKH010M, (b) 688CKE016M, (c) 688CKE025M, (d) 108CKE100MRY, (e) 337CKE200M, and (f) 476CKE400M.

time to failure. According to (42), it has been proven throughout the previous section that the capacity of the capacitor degrades over time. Thus, it is feasible to improve the assessment of the capacitor's reliability by replacing (42) with (11). Therefore, the reliability of the electrolytic capacitor would also be evaluated using (25), which t indicates the time in hours.

$$\begin{aligned}\pi_{\mathrm{CV}} &= 0.32\left(C_{\mathrm{ini}}0.98673\exp(-2t\times10^{-5})\right)^{0.19}\\ &= 0.3192\left((C_{\mathrm{ini}}\exp(-2t\times10^{-5})\right)^{0.19}\\ &\Rightarrow \pi_{\mathrm{CV}}\approx 0.3192\times C_{\mathrm{ini}}^{0.19}\times e^{(-3.8\times10^{-6})t}\end{aligned}\tag{45}$$

$$\begin{aligned}R(t) &= \exp\left[\begin{pmatrix}-8.9376\times10^{-4}\left[\left(\frac{S}{0.55}\right)^3+1\right]\\ \exp\left(4.09\left(\frac{T+273}{358}\right)^{5.9}\right)\end{pmatrix}\right.\\ &\quad\left.\times C_{\mathrm{ini}}^{0.19}\exp\left(-3.8\times10^{-6}t\right)\pi_Q\pi_E t\right]\end{aligned}\tag{46}$$

While it may seem redundant to emphasize the adaptability of the formulation presented in our paper, extending beyond its primary focus on aluminum electrolytic capacitor banks for reliability analysis, it is crucial to underscore its potential for extending its application across diverse capacitor types. This includes a noteworthy emphasis on its relevance within the realm of supercapacitors.

VI. DISCUSSION OF DEGRADATION IN RELIABILITY EVALUATION

It is crucial to highlight the factors contributing to degradation in reliability evaluation. Understanding and addressing these multifaceted causes of degradation is pivotal for developing accurate reliability models and enhancing the longevity and performance of capacitor banks in various applications. One of the primary causes is the gradual reduction in capacitor capacitance over time, stemming from voltage stress, operating temperature, and material quality. Additionally, equivalent series resistance (ESR) and structural integrity are susceptible to degradation, which can be accelerated by environmental conditions like temperature fluctuations and voltage variations. Furthermore, the design and layout of capacitor banks greatly impact degradation rates, underscoring the need to consider these aspects in reliability assessment. This comprehensive understanding of degradation is necessary to make informed decisions, optimize system performance, ensure the safety and reliability of critical systems, and minimize environmental impact and resource waste. Figure 20 shows the reliability variation curves of the individual capacitor banks as a function of failure rate and time (h). As time progresses, reliability decreases, but the effects of degradation (or even other capacitor parameters) become more evident in these curves. The higher the degradation, the lower the capacitor's capacitance, leading to a higher failure rate and ultimately a sharper drop in reliability.

The purpose of such a practical test was to ascertain that the capacitor's capacitance changes over time (the exact magnitude of the degradation was not currently considered). Therefore, this degradation should be accounted for in several areas: 1) When calculating capacitor bank reliability, 2) A reduction in capacitor capacitance means a reduction in the quantity of energy that can be stored in the capacitor, so in storage applications, the degradation in capacitance should be accounted for over time, and it should be specified that after, for instance, 2000 h, a certain amount of energy could be stored in the capacitor bank. 3) As the capacitance degrades, the drop voltage of the CB increases. Therefore, this essential point must be factored into the designs. 4) A reduction of capacitance causes a change in the control speed of the system.

By (14), the reliability of each capacitor is dependent on the λ coefficient on time t, however, the issue is that the degradation of the capacitor λ also changes individually with time, and the degradation is not incorporated into the reliability evaluation relationships. The reliability of capacitors, following (11), is a function of the capacitance C of the capacitor, which is assumed to be always constant. The primary purpose of this article is to modify the reliability assessment relationship by considering the degradation of capacitance. In this manner, (14) is also modified.

The proposed equation offers a distinct advantage over online parameter identification, as it allows for the estimation of reliability, lifetime, and peak current for future CB operations using preliminary parameters such as ESR and capacitance. The key remarks of this paper are as follows:

i) Diverse layouts and designs of CBs, featuring dissimilar voltage, ESR, and output current, result in significantly varied fabrication costs. The meticulous consideration of cost during CB design is crucial, as emphasized in Table 3, where the arrangement of different capacitors leads to a substantial difference in the overall manufacturing cost of CBs.

ii) CB reliability and lifetime are intricately tied to the design and arrangement of capacitors. Higher cost does not necessarily imply longer life, as indicated by the failure rate in Table 4, revealing that an inappropriate CB layout greatly reduces the system's lifetime.

iii) The study explores the impact of PCB or Busbar resistance on the output current of CBs, presenting a new relationship (35) for calculating peak current, considering this type of resistance. This equation is applicable to the calculation of PCB resistance for all CBs.

iv) A comprehensive reliability assessment of CBs based on MIL-HDBK-338B is discussed, considering both short-circuit and open-circuit faults. A novel relationship (20) for calculating CB reliability is presented.

v) The lifetime of a CB is significantly influenced by capacitor voltage and ambient temperature. Tables 6 and 7 demonstrate that a 10° decrease in ambient temperature results in an approximately 33% increase in lifetime, and a 10% decrease in voltage leads to a 21.7% increase in capacitor lifetime.

vi) CBs used in the grid must be designed considering both capacity and output current, necessitating a trade-off between these parameters. In this study, capacitance and output current were separately considered in capacitor bank design, revealing that merely considering capacitance does not provide the current required by the grid.

vii) The peak output current of the CB depends on ESR and capacitor capacitance. laboratory experiments on different capacitors, coupled with the extraction of the formula for capacitance degradation, led to the modification of the formula for calculating the maximum output current of the capacitor.

viii) Through practical experiments and the acquisition of the formula for capacitor degradation, relationships between the calculation of the degradation coefficient and the lifetime of capacitors were improved. Enhanced relationships were also presented for evaluating the reliability and failure rate of a capacitor bank composed of various CBs.

ix) To validate the study's findings, CB design was carried out using seven commercially available CBs,

and experiments on a smaller scale were conducted to examine the degradation of electrolytic capacitors using four different capacitors for 2000 hours.

This paper enhances one of the most widely utilized formulations in the industry for assessing the reliability of power electronic components by incorporating capacitor degradation rates. This addition significantly improves the efficiency and accuracy of the procedure. Furthermore, unlike recent advanced methods that introduce complexity to the system and may deviate from practical applications, our proposed mathematical framework is designed to seamlessly adapt to real experimental scenarios. Its simplicity facilitates accurate assessments over the long-term usage of electronic devices, making it particularly suitable for practical and real-world applications.

VII. LIMITATIONS OF THE STUDY

The degradation trend of capacitors may vary depending on environmental conditions, ripple frequency, ripple amplitude, etc. The MIL-HDBK-217 standard incorporates factors such as system performance environment, quality, ambient temperature, voltage stress (including voltage ripple), and capacitance to assess the reliability of electrolytic capacitors. The capacitance factor degrades over time. To enhance the accuracy of computations, we attempted to derive a coefficient and incorporate it into the calculations of the maximum current, reliability, and lifetime of the capacitor. While the coefficients and relationships presented may not be the most accurate, their inclusion serves to improve the overall accuracy of the calculations.

Another limitation of the study is the comparatively shorter lifetime of semiconductor components in comparison to electrolytic capacitors [53]. The objective of subsequent research is to explore the repercussions of degradation in other inverter components on the performance and longevity of the electrolytic capacitor.

VIII. OPEN QUESTIONS

The CB comprises a combination of series and parallel capacitors, and the impact of an internal capacitor fault on CB reliability and lifetime remains an open question. The lifetime of electrolytic capacitors is more than 2000 (h), but the lifetime of a system that includes all subsystems is reduced to a smaller number. The test performed in this article lasted 2000 (h), which is about 83 days of testing. The possibility of a longer test duration and the consideration of other factors is one of the future goals. However, combining the results of previous different studies (with a capacitor test time of more than 2000 (h)) with the results of our current study is expected to lead to the derivation of the degradation coefficient.

IX. CONCLUSION

The main objective of the work is to incorporate capacitor degradation into the reliability calculations of the CB. Experimental tests were conducted on four electrolytic capacitors for 2000 hours, and the results were recorded to extract the formula for capacitance degradation. Subsequently, the reliability evaluation relationships and the calculation of the maximum output current of the capacitor were modified to account for degradation, leading to the extraction of novel mathematical relationships. Nine common market-available capacitors with different parameters are selected for designing the CB. Using the proposed mathematical framework, reliability analyses, and failure rate calculations are performed to determine the maximum output current of the capacitor over 2000 hours. Additionally, the design of the CB is carried out according to the requirements of a hypothetical microgrid for frequency control. The effects of temperature and voltage stress on capacitor lifetime, as well as the impact of layout design with multiple capacitors on the lifetime and cost of CB construction, are also investigated. Based on the results obtained, the reliability and lifetime of the CB will be improved as follows:

i) Minimize the ambient temperature of the CB as much as practicable.

ii) In capacitor design, aim for minimal voltage stress. MIL-STD-11991 recommends a voltage stress of 0.5 [32].

iii) Select capacitors to constitute the CB in such a way that the CB, with the capability to supply the required current to the grid, has the lowest capacitance.

Consequently, the design of the CB necessitates consideration of both capacitance and ESR degradation. The peak output current, reliability, and lifetime of the CB all depend on the degradation of these factors. When designing a CB, it is not sufficient to consider only capacitance; the ESR and peak output current of each capacitor also need to be considered. The findings also lay the groundwork for future research initiatives:

i) Further investigation into the effects of internal capacitor faults on the reliability and longevity of capacitor banks is warranted.

ii) Exploring the degradation of other components within inverter systems presents a promising area for future research.

iii) Extending test durations beyond 2000 hours and expanding the range of factors under consideration offer exciting directions for future research.

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